Subthreshold Operated CMOS Analytic Model

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***Abstract*—In this paper static and dynamic characteristics analytic models of CMOS circuits operating in subthreshold region are derived. An absolute analogy in behaviour and analysis between strong and weak inversion is shown. Comparation of corresponding parameters in both operation regions is done. Relations between those parameters are derived and their ranges and limitations are treated. Analytic models are verified by PSpice analysis.**

I. Introduction

One of the greatest challenges for every digital system designer is to provide necessary performance along with lowest possible consumption. CMOS circuits certanly represent a good choice. The short circuit dissipation is known to be proportional with V_{DD}^3, while operation speed is proportional to V_{DD}, where V_{DD} is supply voltage. For a long time the consumption decrease and speed increase problems were solved by decreasing the transistor size (scaling) and, consequently, V_{DD} decrease.

In the last decade, the attention of both the researchers and the integrated circuits manufacturers is foucused in CMOS circuits operating in subthreshold region. In this region, V_{DD} is less then the transistor threshold voltage ($V_{DDsub} < V_t$). Thus, the drain current is decreased by several orders of magnitude. This is the reason why short circuit dissipation is decreased by more than 10^5 times. It is also, the reason why the operation speed is decreased by 10^3 times, compared to the strong inversion region [1], [2], [3].

Nevertheless, such significant speed decrease is not always a limiting factor. In practical applications, such as: energy harvester systems, wireless sensor nodes and so on, the CMOS circuits operating in subthreshold region satisfy the speed demands.

Energy harvesting is defined as the conversion of ambient energy present in the environment into electrical energy [4]. The primary interest in the technology derives from its capability to act as an independent power supply for wireless self-powered microsystems, as an alternative to, or to supplement the use of batteries. There are several ways to generate electrical energy locally, such as making use of the kinetic energy of vibrations widely present in the environment, photovoltaic or thermoelectric effects provided there is sufficient incident light or temperature gradient, respectively. Except for vibrations, there are other kinetic energy harvesting applications where the electrical power is generated from foot-strikes, knee bends and backpacks [4].

Wireless sensor nodes (WSNs) can provide information from locations that are inaccessible to the systems that depend on cable connections. WSNs also offer an easy access to information, since it is possible to deploy them in previously unachieveable number of locations [5]. Thus many new application areas are emerging, such as environmental sensing [6], structural monitoring [7], automobile industry [8] and human body monitoring [9]. Because batteries have limited lifetime and are environmentally hazardous, it has become widely agreed that energy harvesters are needed for long-lasting sensor node. The idea is to use energy harvester to capture small amounts of energy from the environment and use the generated energy to power the nodes in wireless sensor networks [5].

Even though the analytic models of the current-voltage characteristics in both strong and weak inversion regions are very different, certain analogies exist. Because of this, CMOS circuits synthesis analogy in both regions is complete. Thus, the developed procedures for system design in strong inversion are used in weak inversion.

In this paper, the analysis analogies between the CMOS circuits in strong and weak inversion regions are shown. Applying the standard current-voltage characteristic equations, analytic models for static and dynamic calculations in subthreshold region are derived. These models include the direct comparation with the corresponding strong inversion parameteres.

II. Current Models

When operating in strong inversion region, well-known simplified MOS transistor current model is used. Thus:

$$I_D = \begin{cases} \mu \frac{C_{ox}}{2} \frac{W}{L} \left[2 \left(V_{gs} - V_t \right) V_{ds} - {V_{ds}}^2 \right], V_{ds} < V_{gs} - V_t \\ \mu \frac{C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_t \right)^2, V_{ds} > V_{gs} - V_t \end{cases} \quad (1)$$

Drain current, when operating in subthreshold region is given by:

$$I_{Dsub} = \begin{cases} I_0 e^{\frac{V_{gs} - V_t}{n \phi_t}} \left(1 - e^{-\frac{V_{ds}}{\phi_t}} \right), V_{ds} < 3\phi_t \\ I_0 e^{\frac{V_{gs} - V_t}{n \phi_t}}, V_{ds} > 3\phi_t \end{cases} \quad (2)$$

where, I_0 represents drain current when $V_{gs} = V_t$ and is given by:

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) {\phi_t}^2. \quad (3)$$

The parameters in Eq. (3) are: μ_0 is carrier mobility, $C_{ox} = \epsilon_{ox}/t_{ox}$ is gate oxide capacitance (ϵ_{ox} is the dielectric constant and t_{ox} is the gate oxide thickness), W and L are channel width and length, V_t is threshold voltage, $\phi_t = kT/q$ is temperature potential ($\phi_t = 26mV$ at $300K$), and $n = 1 + C_d/C_{ox}$ is the subthreshold slope factor.

According to Eq. (2), when $V_{ds} > 3\phi_t = 78mV$ drain current I_{DDsub} does not depend on drain-source voltage (V_{ds}), because $e^{-3} << 1$, while this dependance is exponential when $0 \leq V_{ds} \leq 3\phi_t$, Fig. 1. Thus, analogous to the strong inversion region operation, in subthreshold there are two regions of the $I_{DDsub} = f(V_{ds})$ characteristic: saturation region ($V_{ds} > 3\phi_t$) and non-saturation region ($0 \leq V_{ds} \leq 3\phi_t$). The difference is that the drain current is a quadratic function of the drain-source voltage in strong inversion (V_{ds} in nonsaturated region and V_{gs} in saturated region), while in subthreshold this function is exponential ($I_{DDsub} \sim e^{V_{ds}}$ in non-saturated and $I_{DDsub} \sim e^{V_{gs}}$ in saturated region). This shows that there is a complete analogy between CMOS circuits in strong and weak region synthesis and analysis.

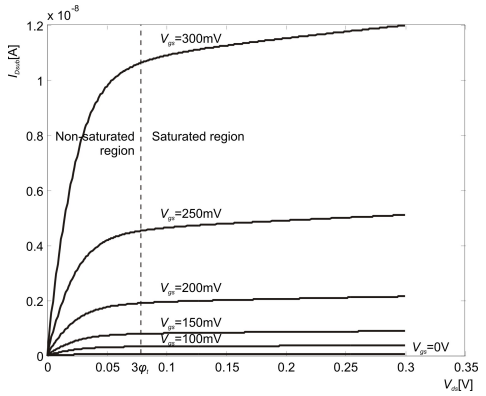

Fig. 1. $I_{Dsub} - V_{ds}$ characteristics in subthreshold operation region

III. Static Characteristics

In Fig. 2a CMOS inverter is shown. Operation region depends on the relation between supply voltage V_{DD} and NMOS and PMOS threshold voltages, V_{tn} and V_{tp}. In this paper, we assume $V_{tn} = |V_{tp}| = V_t$. The transistor operates in strong inversion when $V_{DD} > V_{tn} + V_{tp} = 2V_t$, while it operates in in subthreshold region when $3\phi_t < V_{DD} < V_t$, Fig. 2b. For low values of V_{DDsub}, drain current I_{DDsub} is very low. Thus, the output voltage rise and fall time intervals are extremely long. Subthreshold region threshold voltage V_{tsub} can be defined as the voltage V_{gs} at which the drain current is equal to $0.01I_0$, Fig. 2b. Thus, based on Eq. (3):

$$V_{tsub} = V_t - 4.6n\phi_t. \quad (4)$$

According to Eq. (4), supply voltage practical values in subthreshold operation region are:

$$V_t - 4.6n\phi_t < V_{DDsub} < V_t. \quad (5)$$

When trasistor operates as a switch, it is considered turned off at $V_{gs} < V_{tsub}$ and turned on at $V_{tsub} < V_{gs} < V_{DD}$.

CMOS inverter threshold voltage V_T and its maximum current I_{DDM} from the supply voltage in switching region are, respectively, given by:

$$V_T = V_t + \frac{V_{DD} - 2V_t}{1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}, \quad (6)$$

$$I_{DDM} = \mu_n \frac{C_{ox}}{2} \frac{W}{L} \frac{(V_{DD} - 2V_t)^2}{\left(1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}\right)^2}, \quad (7)$$

where NMOS and PMOS channel lengths are equal $L_n = L_p$.

CMOS inverter operating in subthreshold region transfer characteristics, both voltage and current, are shown in Fig. 2. Threshold voltage V_{Tsub} in subthreshold is obtained, in the same way as in strong inversion, by equalizing currents $I_{Dnsub} = I_{Dpsub}$ in the saturated region of the characteristic, i.e.:

$$I_{0n} e^{\frac{V_i - V_t}{n\phi_t}} = I_{0p} e^{\frac{-V_i + V_{DD} + V_t}{n\phi_t}}. \quad (8)$$

Replacing $V_i = V_{Tsub}$ in Eq. (4), and solving by V_{Tsub}, we obtain:

$$V_{Tsub} = \frac{V_D Dsub}{2} - \frac{n\phi_t}{2} ln\left(\frac{I_{0n}}{I_{0p}}\right). \quad (9)$$

If the inverter is symmetric, i.e. if:

$$\frac{I_{0n}}{I_{0p}} = \frac{\mu_{0n} \frac{W_n}{L_n}}{\mu_{0p} \frac{W_p}{L_p}} = 1, \quad (10)$$

threshold voltage is given as $V_{Tsub} = V_{DDsub}/2$. Threshold voltage of the symmetric CMOS inverter operated in strong inversion region is also $V_T = V_{DD}/2$.

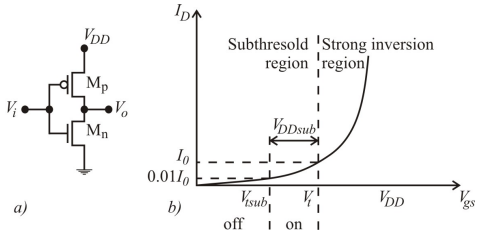

Fig. 2. CMOS inverter (a) and MOS transistor $I_D - V_{gs}$ characteristic

Supply voltage current is given as:

$$I_{DDMsub} = \begin{cases} I_0 n e^{\frac{V_i - V_t}{n\phi_t}}, & 0 \leq V_i \leq V_{Tsub} \\ I_0 p e^{\frac{-V_i + V_{DDsub} + V_t}{n\phi_t}}, & V_{Tsub} \leq V_i \leq V_{DDsub} \end{cases} \quad (11)$$

Maximum value of I_{DDsub} is obtained at $V_i = V_{Tsub}$, so:

$$I_{DDMsub} = I_{0n} \sqrt{\frac{I_{0p}}{I_0 n}} e^{\frac{V_{DDsub}/2 - V_t}{n\phi_t}} \quad (12)$$

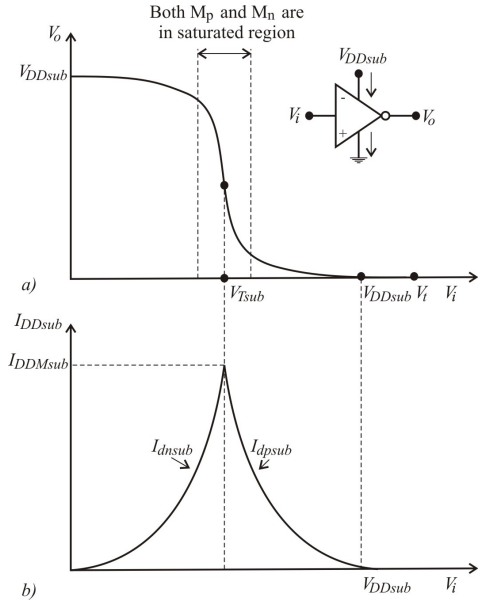

Fig. 3. CMOS inverter operating in subthresold region $V_0 = V_i$ (a) and $I_{DDsub} - V_i$ (b) static characteristics

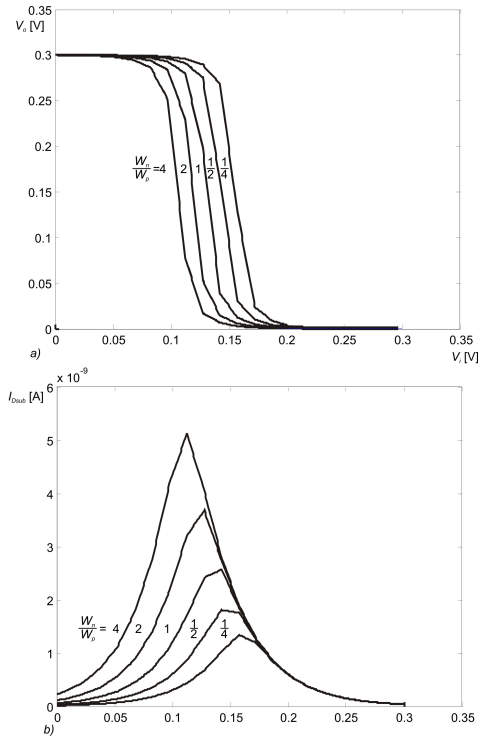

Fig. 4. CMOS inverter operating in subthreshold region voltage (a) and current (b) transfer characteristic, where the ratio W_n/W_p is varied for the same $L_n = L_p$

If the inverter is symmetric, Eq. (10), then:

$$I_{DDMsub} = I_{0n} e^{\frac{V_{DDsub}/2 - V_t}{n\phi_t}} \tag{13}$$

Maximum currents ratio of the CMOS inverter in the short

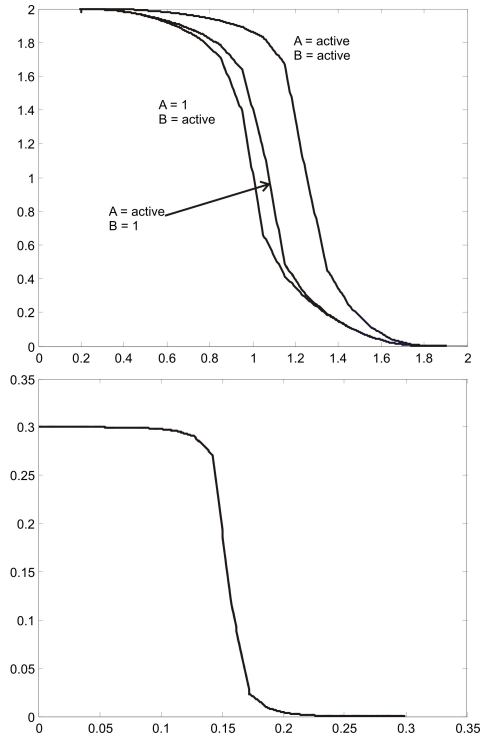

Fig. 5. NAND2 $V_o - V_i$ static characteristics as a function of the number of active inputs, operating in strong (a) and weak (b) inversion region

circuit area, according to Eqs. (7), (10) and (13) is given by:

$$\frac{I_{DDMsub}}{I_{DDMsub}} = \frac{(V_{DD} - 2V_t)^2}{8\,(n+1)\,{\phi_t}^2} e^{\frac{V_t - V_{DDsub}/2}{n\phi_t}}. \tag{14}$$

For example, at $V_t = 500mV$, $V_{DD} = 2V$, $V_{DDsub} = 350mV$ and $n = 1.5$, we obtain $I_{DDM}/I_{DDMsub} = 0.22 \times 10^6$. In general, we can say that strong inversion maximum current I_{DDM} is greater than subthreshold maximum current I_{DDMsub} by 10^4 to 10^6 times.

Eqs. (9) and (13) show that the threshold voltage and the maximum current of the CMOS inverter supply voltage while operating in subthreshold region depend on the transistor geometry ratio $(W_n/L_n)/(W_p/L_p)$. Such claim is confirmed by static characteristics obtained by PSpice analysis, Fig. 2.

Threshold voltage V_T, Eq. (6) and current I_{DDM} in strong inversion region also depend on the ratio $(W_n/L_n)/(W_p/L_p)$. With this, the functional analogy between the strong and weak inversion region is confirmed, when basic static parameters are cosidered.

NAND and NOR circuits threshold voltages depend on the number of inputs, number of active inputs and the combination of the active inputs. In subthreshold operation region, this dependence is negligible for two reasons. First, supply voltage is very low (a few hundreds of mV). Second, V_{tsub} is a logarithmic function of W_n/W_p, multiplied by a small voltage ($n\phi_t \sim 40mV$). Thus, the sensitivity to change is much lower than when transistor operates in the strong inversion region, Fig. 5.

IV. Dynamic Model

In Fig. 6a CMOS inverter and its parasitic capacitances are shown and in Fig. 6b, its model for switching process analysis is shown. In [10] capacitances C_{gsp} and C_{gdn} are mapped to the input and to the output, but with capacitance values doubled:

$$\begin{aligned} C_I &= C_{gsn} + C_{gsp} + 2\left(C_{gdn} + C_{gdp}\right) \\ C_O &= C_{dsn} + C_{dsp} + 2\left(C_{gdn} + C_{gdp}\right) \\ C_L &= C_O + NC_I \end{aligned} \tag{15}$$

where N is the fanout number.

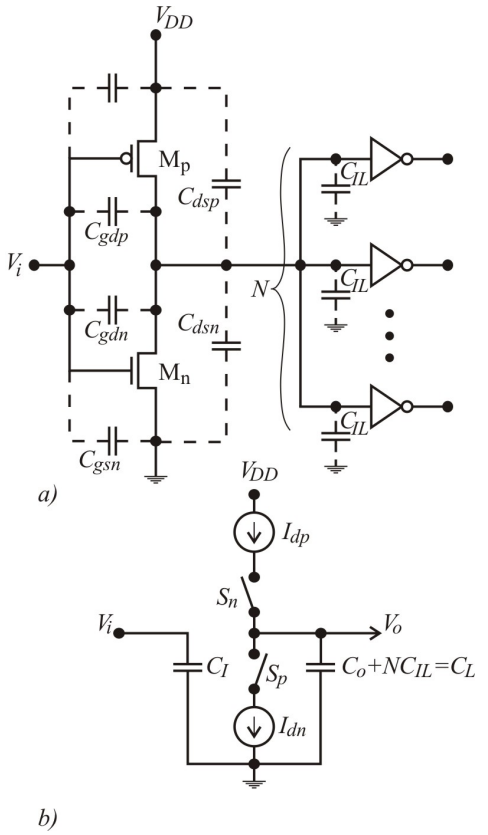

Fig. 6. CMOS inverter with corresponding capcitances (a) and its dynamic model (b)

At step input voltage, when changing from 0 to V_{DD}, PMOS transistor is turned off (S_p off) and NMOS is turned on (S_n on), so the capacitor C_L is discharged by the current I_{dn} The transistor M_n is first in saturated region and then in non-saturated region.

Output voltage fall time t_{pHL} of CMOS inverter operating in strong inversion region is given by:

$$t_{pHL} = \frac{C_L}{\beta_n\left(V_{DD} - V_{tn}\right)}\left(1.45 + \frac{V_{tn}}{V_{DD} - V_{tn}}\right). \tag{16}$$

On the falling edge of the input voltage, i.e. change from V_{DD} to 0, causes M_n to be turned off (S_n off) and M_p turned on (S_p on). Thus, C_L is charged by the current I_{Dp}, so the output voltage rise time is given by:

$$t_{pLH} = \frac{C_L}{\beta_n\left(V_{DD} + V_{tp}\right)}\left(1.45 + \frac{|V_{tp}|}{V_{DD} - V_{tn}}\right). \tag{17}$$

Working point trajectory of the transfer regime in subthreshold region is shown in Fig. 7. Capacitor C_L discharhing I_{Dnsub} and charging I_{Dpsub} currents, are given by:

$$I_{Dnsub} = I_{0n} e^{\frac{V_{DDsub} - V_{tn}}{n\phi_t}} \tag{18}$$

$$I_{Dnsub} = I_{0p} e^{\frac{V_{DDsub} + V_{tp}}{n\phi_t}} \tag{19}$$

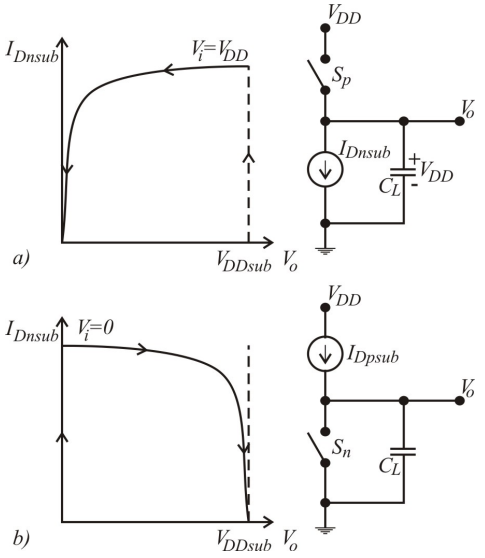

Fig. 7. Working points trajectory and the equivalent circuits to charge (a) and discharge (b) C_L, when operating in subthreshold region

Since in saturated region $V_{ds} < 3\phi_t$, we can assume that the switching regime is finished when the working point enters the non-saturated region. The switching regime is defined by the C_L charge and discharge time intervals. If the inverter is symmetric ($I_{0n} = I_{0p}$, $V_{tn} = |V_{tp}| = V_t$), the time intervals t_{pHL} and t_{pLH} are equal and are given by:

$$t_{pHLsub} = t_{pLHsub} = C_L \frac{V_{DD}}{I_0} e^{\frac{V_t - V_{DDsub}}{n\phi_t}}. \tag{20}$$

Input pulses period has to satisfy the condition given by:

$$T_{sub} \geq t_{pHLsub} + t_{pLHsub} = 2C_L \frac{V_{DD}}{I_0} e^{\frac{V_t - V_{DDsub}}{n\phi_t}}. \tag{21}$$

Inverter maximum working frequency is given by:

$$F_{maxsub} = \frac{1}{T_{minsub}} = \frac{I_0}{2C_L V_{DD}} e^{-\frac{V_t}{n\phi_t}} e^{\frac{V_{DDsub}}{n\phi_t}}. \tag{22}$$

When operating in strong inversion region, F_{max} is a linear function of the supply voltage (Eqs. (16) and (17) and Fig. 8a). In subthreshold region, this function is exponential (Eqs. (22) and Fig. 8b).

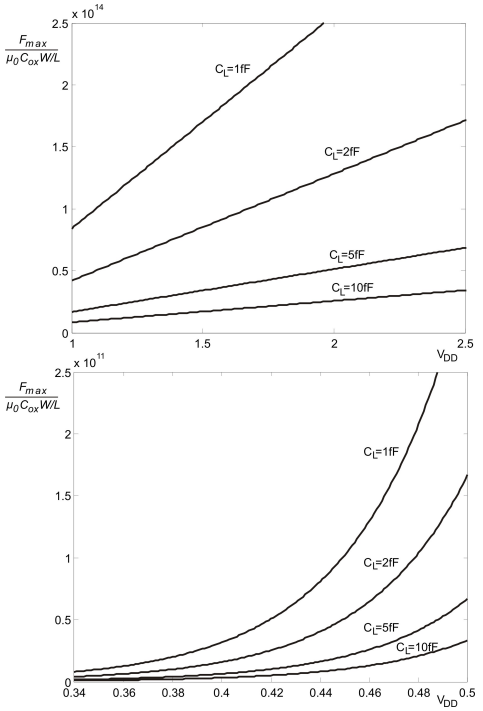

Fig. 8. Normalized F_max as a function of V_{DD}, shown for different values of C_L, when operating in strong (a) and weak (b) inversion region

V. Dissipation

Static dissipation in both operation regions is obtained when supply voltage V_{DD} and junction leakage current I_{DSS} are multiplied, i.e.:

$$P_{DDS} = V_{DD} I_{DSS} \tag{23}$$

Dynamic dissipation is calculated as mean value of the transistor dissipation during one cycle of the step input voltage. It is a consequence of the C_L charging and discharging when in switching regime. The capacitor C_L is charged by the current I_{Dp} PMOS and discharged by the current I_{Dn} of the NMOS transistor. Since these currents are given by:

$$I_{Dp} = C_L \frac{dV_o}{dt}, I_{Dn} = -C_L \frac{dV_o}{dt}, \tag{24}$$

we obtain:

$$\begin{aligned} P_{DD} &= \frac{1}{T}\left[\int_0^{T/2} V_o(t)\, I_{Dn}(t)\, dt + \right. \\ &\left. + \int_{T-T/2}^{T} (V_{DD} - V_o(t)\, I_{Dp}(t)\, dt\right] = \\ &= C_L V_{DD} f, \end{aligned} \tag{25}$$

where $f = 1/T$ represents the input pulses frequency.

Thus, dynamic dissipation, in both operating regions, is proportional to ${V_{DD}}^2$. Since V_{DD} in strong inversion region is several times greater than V_{DDsub} in subthreshold, the dyanmic dissipation is also greater by several tens when compared to the dissipation in subthreshold region.

The above analysis is valid when ideal input voltage and ideal MOS transistors are considered. In practice, there are always input voltage rise and fall times. These are the reason why, at certain intervals, both transistors are turned on, causing additional dissipation. Thus, this dissipation is dubbed short circuit dissipation.

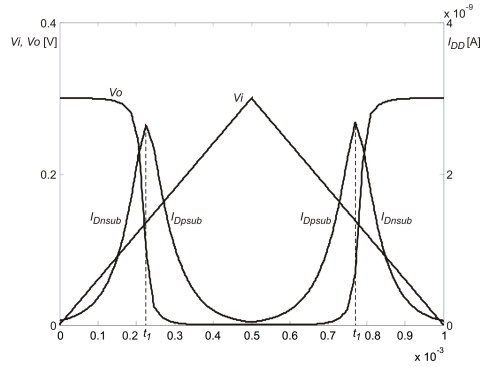

Fig. 9. Supply voltage current response to an input voltage linear change, when operating in subthreshold

CMOS inverter short circuit dissipation, when operating in strong inversion region and when the input voltage is a linear function of time, is given by [10]:

$$P_{dsc} = \frac{1}{3} I_{DDM} (V_{DD} - 2V_t)(t_r + t_f) f, \tag{26}$$

where t_r and t_f are the input voltage rise and fall times, and I_{DDM} is given by Eq. (7). Since I_{DDM} is a quadratic function of V_{DD}, then $P_{dsc} \sim {V_{DD}}^3$.

Supply voltage current response in subthreshold region to an input voltage linear change is shown in Fig. 9. Dissipation mean value during one cyvle is given by:

$$P_{dsc} = \frac{1}{T}\int_0^T V_{DDsub} i_{DDsub}(t)\, dt. \tag{27}$$

If the inverter is symmetric, then $I_{dnsub} = I_{dpsub}$. Thus, the dissipation is equal for all periods: $0 - t_1, t_1 - T/2, T/2 - t_2$ and $t_2 - T$. Further, we have:

$$\begin{aligned} P_{dsc} &= 4\frac{V_{DDsub}}{T}\int_0^{t_1} I_{Ddnsub}(t)\, dt = \\ &= 4\frac{V_{DDsub}}{T} I_{0n}\int_0^{t_1} e^{\frac{St - V_t}{n\phi_t}} dt, \end{aligned} \tag{28}$$

where $S = dV_i/dt$ represents the input voltage slope changes. When the input signal is symmetric, we have: $t_r = t_f = V_{DD}/t_r$, where t_r and t_f are time intervals of the input voltage rise and fall times. Solving Eq. (28), yields:

$$P_{dsc} = 4n\phi_t I_{DDMsub} t_r f, \tag{29}$$

where I_{DDMsub} is given by Eq. (13). If the input voltage change is asymmetric ($t_r \neq t_f$), we obtain:

$$P_{dscsub} = 2n\phi_t I_{DDMsub}(t_r + t_f) f, \tag{30}$$

We have $P_{dsc} \sim {V_{DD}}^3$ while operating in strong inversion region and $P_{dscsub} \sim {\phi_t}^3 e^{V_{DDsub}}$ in subthreshold region.

Thus, we obtain $P_{dscsub} << P_{dsc}$. If the inverter is symmetric, Eqs. (26) and (29) yield:

$$\frac{P_{dsc}}{P_{dscsub}} = \frac{\left(V_{DD} - 2V_t\right)^3}{48n\left(n-1\right){\phi_t}^3} e^{\frac{V_t - V_{DDsub}/2}{n\phi_t}}. \qquad (31)$$

For example, if $V_{DD} = 2V, V_t = 0.5V, n = 1.5$ and $V_{DDsub} = 360mV$, we calculate $P_{dsc}/P_{dscsub} \sim 4.7 \times 10^6$.

VI. Conclusion

Analysis results show complete analogy in behaviour of strong and weak inversion region. CMOS logic circuits static and dynamic parameters functional dependence in both operation regions is also shown. Logic circuits threshold voltage depends on, besides the supply voltage, transistor geometry. The threshold voltage is inversely proportional to this ratio, while operating in strong inversion region. When operating in subthrehold region, threshold voltage is proportional to the logarithm of this ratio. In both operation regions, threshold voltage of the symmetric inverter is equal to half the supply voltage. NAND and NOR circuits static transfer characteristic almost does not depend on the number of active inputs. When operating in strong inversion, short circuit dissipation is proportional to ${V_{DD}}^3$. When operating in subthreshold, short circuit dissipation is proportional to ${\phi_t}^3 e^{V_{DDsub}}$. Thus, subthreshold dissipation is 10^5 to 10^6 times less than the strong inversion dissipation.

Maximum inverter operation frequency, while operating in subthreshold, is 10^3 to 10^4 times less than frequency while operating in strong inversion region. This frequency is proportional to $e^{V_{DDsub}}$ in subthreshold, and to V_{DD} in strong inversion region.

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