Parametric SPICE Model for Static Induction Transistor (SIT) in triode mode of operation

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***Abstract*—The static induction transistor (SIT) is a device which belongs to the multichannel power FET family. Depending on its internal source resistance it can achieve triode or pentode like output characteristics. The purpose of this work is to present a simple model suitable for computer analysis and simulation of circuits containing SITs in triode-like mode of operation. The model is based on the SITs static and dynamic behaviour, and not on the physical structure and characteristics of the device. A possible method for extraction of the model parameters is proposed. The simulated static and frequency characteristics correspond well to the experimental results available from the references. The model has passed all performed tests. Although the proposed model is not yet an ideal solution it will help to start simulating circuits containing the static induction transistors for different applications.**

Keywords—Static induction transistor (SIT); static characteristics; SPICE; modeling; parameter extraction

I. Introduction

The basic principles of the field-effect transistor (FET) were described by J. E. Lilienfeld [1] - [3], while the theoretical analysis was performed by W. Shockley in 1952 [4]. In early 1950's there were two main goals which occupied the scientists dealing with further development of the FET. The first one was a creation of semiconductor device with triode-like *I-V* characteristics and the other was the development of high power device based on field effect principles – power FET. In 1950 Y. Watanabe and J. I. Nishizawa, investigating the possibilities of creating semiconductor device with triode like characteristics have developed the concept of vertical "analog" transistor [5], while in 1952 W. Shockley proposed the, so-called, "analog transistor" [6]. It was shown that the saturation region in the FET's *I-V* characteristics is a result of the internal negative feedback caused by the series channel resistance (r_s). As a result the FET's overall transconductance (G_m') changes to value [7]

$$G_m' = G_m/(1+ r_s \cdot G_m). \quad (1)$$

For $r_s \cdot G_m >> 1$ (1) reduces to:

$$G_m' \approx 1/r_s \quad (2)$$

On the other hand, if $r_s \cdot G_m << 1$ in the entire region, (1) becomes

$$G_m' = G_m, \quad (3)$$

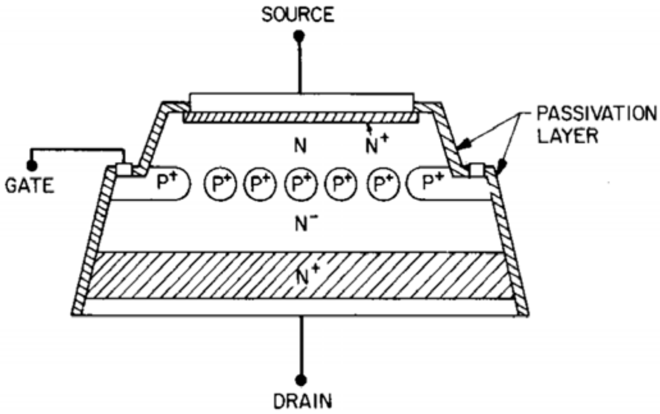
and the device will not exhibit saturation. Instead, its characteristics will be triode-like.

The research considering the development of power FETs resulted in similar conclusions. Namely, any power semiconductor device should have large current carrying capabilities, low power losses in conducting mode of operation, and high blocking voltage in non conducting mode. These imply very short and as wide as possible device channel. The first attempt in creating power FET was the "cylindrical field-effect transistor", proposed by H. A. R. Wegener [8] in 1959. It was clear, from the beginning, that the width of the channel cannot be increased, without losing part of the wanted device characteristics, beyond certain critical value. The main problem was the control of the channel width for very short channel device. Possible solutions of this problem were proposed by R. Zuleeg [9] − [12] and his "Multichannel field–effect transistor", as well as by S. Teszner and R. Gicquel [13] and their "Gridistor". Both components are based on the vertical multichannel structure where many vertical channels are connected in parallel forming "parallel multichannel FET". Due to the very short channel these devices could operate, depending on their gate-to-source voltage, in both: triode-like and pentode-like mode of operation. Unfortunately, these devices did not find any commercial applications.

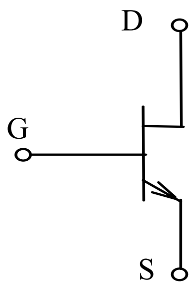
II. The Static Induction Transistor (SIT)

Knowing the pros and contras of the multichannel FETs and gridistors, in 1975 J. Nishizawa and his associates have proposed a device based on previous two. As it was made clear that the main mechanism of operation of this device is based on the static induction it was named "static induction transistor" – SIT [14] − [16]. According to its output *I-V* characteristics SIT can be considered as a solid-state analogy of the vacuum tube, which, at certain predefined pinch-off voltage, can be operated in triode-like and/or pentode-like mode of operation. Basically, SIT can be considered as a multichannel structure (Fig. 1) which, when no voltage is applied to the gate, is in the on-state.

The main characteristics of the SIT, in triode mode of operation, are: very short channel length, low internal series resistance, low input (gate to source) capacitance, low noise, low harmonic distortions, and possibility to control high power at audio-frequencies. The transient on/off time is very short (typically around 250 ns). SIT exhibits relatively high voltage drop in forward conducting state (90 V for 180 A device, and 18 V for 18 A device). It's current and voltage ratings can exceed 300 A and 1200 V, respectively. SIT's operating frequency can be higher than 100 kHz which makes it very suitable for high-frequency high-power applications (audio, VHF, UHF and microwave amplifiers). The very first commercial SIT's were fabricated by *Tokin Corporation* of Sendui, Japan [17]. Today, SIT became very popular for audio applications as building devices in A-class power audio-amplifiers. Namely, the triode-like SIT becomes an ideal replacement for the vacuum triode, commonly used in these applications [18]. Nowadays, several companies already produce SIT-based audio-amplifiers.



(a)



(b)

Figure 1. Basic structure of SIT and device symbol: a) basic structure [18]; b) device symbol

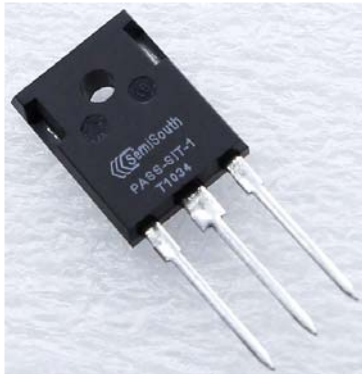


Figure 2. SIT manufactured by SemiSouth [19]

One of them is *Digital Do Main* from Japan, which uses SIT's fabricated by *Yamaha Silicon*. Another one is *First Watt*, that fabricate audio-amplifiers based on SiC SIT's produced by *SemiSouth Company* as an "application specific device" for this purpose (Fig. 2) [19].

The typical SIT's (triode-like and pentode-like) *I-V* output characteristics are presented in Fig. 3.

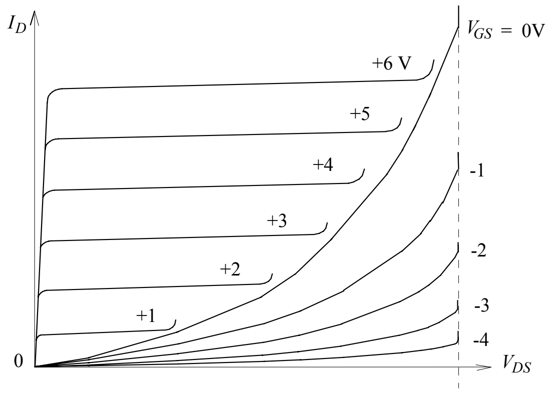


Figure 3. Typical SIT output *I-V* characteristics

III. SIT Modeling

Electronic circuit design requires accurate methods of evaluating circuit performance. Today, because of the enormous complexity of modern electronic circuits, in this process, the computer aided circuit analysis and simulation are essential and can provide information about circuit performance that is almost impossible to obtain with laboratory prototype measurements. Since the appearance of the SIT numerous attempts have been made to develop appropriate device models suitable for theoretical, but also computer aided, analysis and simulation of the SIT based systems [20] – [28]. Some of these models are pure analytical and are based on the physical laws governing the SIT behaviour. However, only few of them are adapted to computer programs for analysis and simulation [22] (PSpice), [25] (Saber). Unfortunately, all of these models are based on pentode-like (bipolar) SIT mode of operation. In lack of triode-like SIT models for circuit analysis and simulation and having into consideration the increasing interest for this device in designing the output stages of audio-amplifiers [19], a simple parametric model suitable for Spice based simulations is presented below.

A. Spice Models for Vacuum Triode

The first approach was to modify the Spice models for vacuum triode based on the well-known Child-Langmuir law (known also as space-charge conduction law). The basic model was proposed in [29]. As it was not applicable for real triodes some improvements were presented in [30]. The improved model [30] is based on the behaviour of the vacuum triode and is not supported by its physical laws. Considering the fact that the SIT's output characteristics are based on static induction and that they follow the exponential law rather than the space-charge conduction law, the final conclusion was that these approach cannot be easily modified into triode-like SIT model. On the other hand, when trying to use the derived formulas [14], [15] and [31] in SIT modeling the main problem to solve was the model parameter extraction, as these values are dependent of the physical parameters and/or behaviour of the device. Therefore other possibilities had to be investigated.

B. Spice Model for SIT in triode-like mode of operation

In 2013 the simple model for triode-like N-channel SIT was proposed [32]. The model is quite simple and is based on the results in modeling the static induction thyristor [33]. The model was developed using the analog behavioral modeling, available in any modern version of Spice, and is based on SIT's static and dynamic behaviour, rather than on its physical structure.

The schematic structure of this model for an N-channel device is presented in Fig. 4.

The model is consisted of three voltage-controlled voltage sources (VCVS), two diodes, two resistors and one capacitor. Additionally three capacitors (C_{GS}, C_{GD} and C_{DS} – not shown in Fig. 4) can be added for better modeling of the SIT's frequency response.

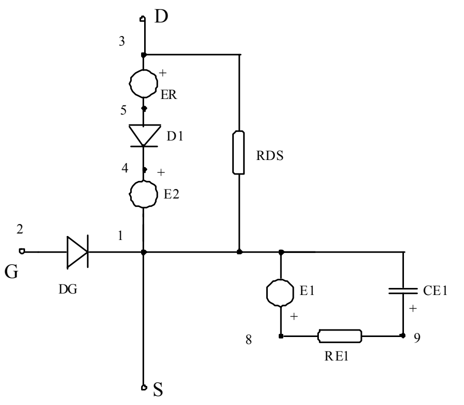


Figure 4. N-channel Spice model for triode-like SIT

Figure 5 presents the subcircuit definition for the model from Fig. 4. The **.param** function allows easy entering necessary model parameters.

```
.param  p=p q=q rs=rs n=n is=is re1=re1 ce1=ce1

.subckt sit      3    2    1
*-------------- D    G    S
er  3 5 value = {v(4,1)*v(5,4)}
d1 5 4 d1
.model d1 d(rs= rs is= is n= n)
e2 1 4 9 1 1
rds 3 1 24meg
dg 2 1 d2
.model d2 d(rs=.3 is=1e-6)
e1 8 1 value = {((v(2,1)* p)*(( q –v(2,1)))}
re1 8 9 re1
ce1 9 1 ce1
.ends
```

Figure 5. Subcircuit definition for the SIT model from Fig. 4

The diode D_G is used to simulate the *pn* junction nature of the gate. While simulating the triode-like mode of SIT operation this diode should be reverse biased. The main current path is composed of two VCVS (E_R and E_2) and the diode D_1.

The VCVS E_R is used for modeling the shape of the SIT's output *I-V* characteristics. Its voltage is actually influenced by the voltages across the VCVS E_2 and the diode D_1.

Besides, the VCVS E_2 serves to define and implement the knee of any single curve in the output characteristics. Namely, although this characteristic value depends on several factors it can be estimated as:

$$V_{B,DS} \approx |V_{GS}| \cdot p \cdot \left(q + |V_{GS}|\right) \tag{4}$$

where *p* and *q* are parameters which can be obtained by simple measurements of two curves in the family of the output characteristics for the value of the current of 5mA.

In this model the diode D_1 has several tasks: (1) it provides the forward conducting and the reverse blocking characteristics of the device; (2) by adjusting the parameters **rs** (internal diode resistance), **is** (reverse saturation current) and **n** (diode emission coefficient) in the Spice diode model, the internal resistance of the device and the slope of the output characteristics can be modeled. In [32] the curve fitting was performed by trial and error and after several iterations the values were satisfactory determined. But, knowing that, in the proposed model, the drain to source voltage is defined by E_R, D_1 and E_2 as:

$$\begin{aligned} V_{DS} &= V_{GS} \cdot p \cdot \left(q - V_{GS}\right) + \\ &+ \left(\frac{T}{11605} \cdot n \cdot \ln \frac{I_D}{I_s} + r_s \cdot I_D\right) \cdot \left[1 + V_{GS} \cdot p \cdot \left(q - V_{GS}\right)\right] \end{aligned} \tag{5}$$

which, for V_{GS}=0 (5) becomes:

$$V_{DS} = \frac{T}{11605} \cdot n \cdot \ln \frac{I_D}{I_s} + r_s \cdot I_D \tag{6}$$

It is easy to calculate *n* as:

$$n = \frac{V_{DS} - r_s \cdot I_D}{T/11605} \cdot (\ln \frac{I_D}{I_s})^{-1} \quad . \qquad (7)$$

For all parameter calculations, the working temperature of the device was assumed to be 350 K.

The value of the diode internal resistance r_s, in ohms, can be estimated as:

$$r_s \cong \sqrt{\frac{\Delta V_{DS}}{\Delta I_D}} \qquad (8)$$

In all simulations the value of the diode reverse saturation current was chosen to be 10^{-6}A.

The circuit consisted of VCVS E_1, resistor R_{E1} and the capacitor C_{E1} is, essentially, used to model the device AC characteristics. Additionally, in this case, it is used also to adapt the gate control function before including its influence into the main current path through VCVS E_R. It should be noted that during the AC analysis the value of R_{E1} is to be equal to the value of the load drain resistance in the analyzed circuit.

Although the explained model is valid for the N-channel SIT, its modification for simulating P-channel devices should not be a problem.

IV. Simulation Results

Extensive simulations have been performed in order to test the proposed model characteristics. The model has passed all performed tests and can be used to analyze various types of power converters using SI transistors. In lack of real device the simulation results are compared with the measured results for real SITs, presented in [14], [15], [19] and [31]. All simulations were performed using Spice versions produced by two different companies: (1) Pspice Lite v16.6 - Cadence Design Systems Inc. [34] and (2) LTspice v4.12t - Linear Technology Corporation [35]. Only few of the obtained results are presented below.

A. Simulation Results - DC Mode of Operation

Several types of SIT were modeled and their models were tested using both of the above mentioned Spice programs. For each example of SIT its model parameters were extracted from its measured characteristics using equations (4), (7) and (8). In Fig. 6 the measured [14] and simulated I_{DS}-V_{DS} static characteristics (using the model presented in Fig. 4), for 1000 V SIT (fabricated by Tokin Corporation), are presented. Although there is a visible discrepancy between the curves for V_{gs}=0, which is caused by the relatively high value of the parameter **rs** in the diode model, it can be seen that for all other values of V_{gs} the simulated results correspond well with the measured ones.

The simulated I_{DS}-V_{DS} static characteristics, for the 40 V SIT (2SK76) produced by Tokin Corporation, are presented in Fig. 7-b. Model parameters were extracted from the measured characteristics given in Fig. 7-a [15], using the method described above. Again, the simulated results correspond well to the measured ones.

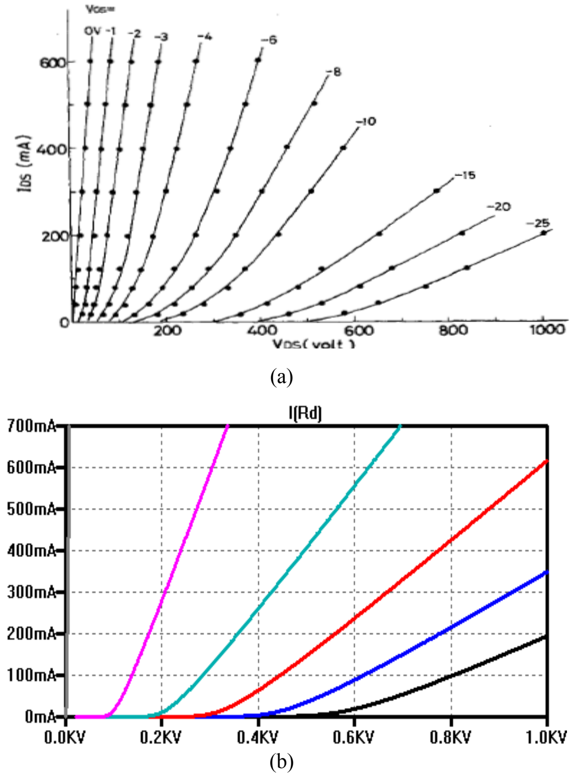


Figure 6. 1000 V SIT (Tokin Corp.) I_{DS}-V_{DS} characteristics: a) measured characteristics [14]; b) simulated characteristics using model from Fig. 4 with p=0.0714, q=100, rs=8Ω, n=6, is=10^{-6}A (V_{DS} is on the horisontal axis; I_D is on the vertical axis; V_{GS} was changed from 0 to -25 V in steps of -5 V.)

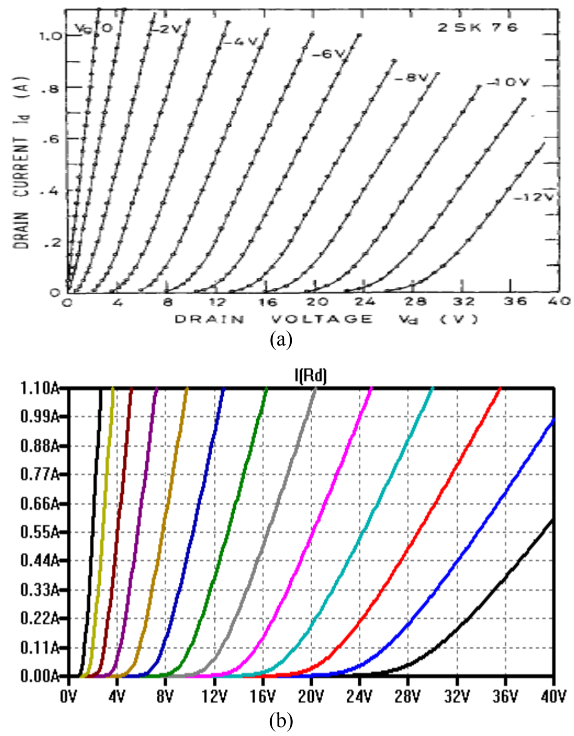


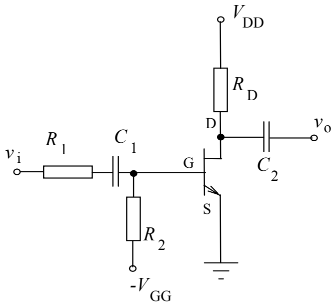
Figure 7. 40 V SIT (2SK76) I_{DS}-V_{DS} characteristics: a) measured characteristics [15]; b) simulated characteristics using model from Fig. 4 with p=0.0694, q=3, rs=1.1Ω, n=4, is=10^{-6}A (V_{DS} is on the horisontal axis; I_D is on the vertical axis; V_{GS} was changed from 0 to -12 V in steps of -1 V.)

B. Simulation Results – Frequency Response

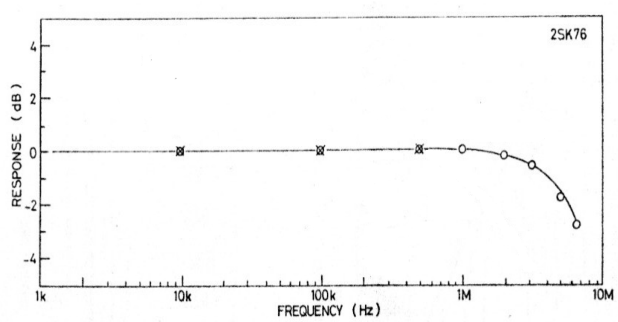
It has already been said that one of today's main applications of triode-like SIT is in building linear audio-amplifiers. Therefore, the frequency response (small signal operation) of the proposed model has, also, been tested. The simulation of the frequency response, for the improved 2SK76 SIT [31], was performed using the same circuit topology (Fig. 8-a) as in [31] with the load resistance of 8 ohms. Equation (9) is used to adjust the high frequency amplitude response of the model to that of the practical device, shown in Fig. 8-b [31]. In (9) R_{E1} should have the same value as R_D so the only unknown remains C_{E1}.

$$f_H = 1/(2\pi R_{E1} C_{E1}) \qquad (9)$$

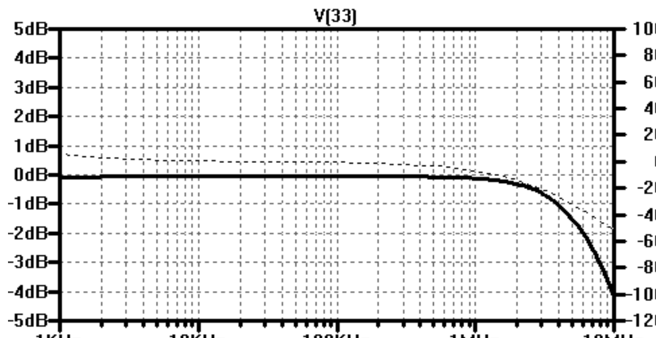
The results are shown in Fig. 8-c. The upper cut-off frequency of 8 MHz has been obtained for C_{E1} =2.5 nF. It can be seen that the simulated curve correspond well to the measured one.



(a)



(b)



(c)

Figure 8. SIT Frequency amplitude response (improved 2SK76): (a) circuit; (b) measured amplitude response from [31]; (c) simulated response using: C_{E1} =2.5 nF, $R_{E1} = R_D$=8Ω, p=0.0694, q=3, rs=1.1Ω, n=4, is=10^{-6}A. (V(33)≡v_o – the solid line shows the amplitude response while the dashed line shows the phase response)

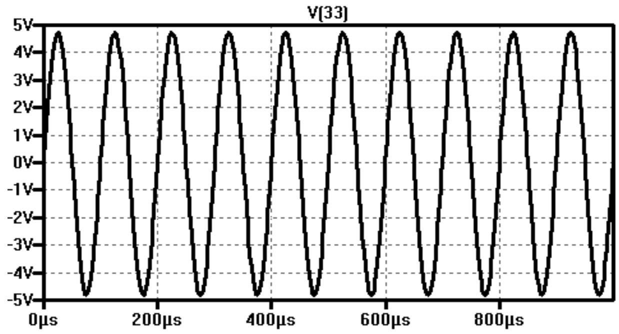


Figure 9. The output voltage (v_o) waveform – the magnitude of the input sinewave voltage is chosen so that the delivered power to the 8Ω load is 1.5W. The SIT model parameters are (100 V SIT): p=0.0714, q=100, rs=8Ω, n=6, is=10^{-6}A (the signal frequency is f_i = 10kHz, while R_D=8Ω, C_1 = 10µF, C_2 = 100µF)

To examine the linearity of the model transfer characteristics the common source configuration from Fig. 8-a was used. The AC voltage source was connected to the gate of the device through the 10 µF capacitor. The load (R_L = 8 Ω) was connected to the drain of the SIT through 100 µF capacitor. The magnitude of the input sine-wave signal was chosen so that the power of 1.5 W was delivered to the load [19]. The simulated output voltage is shown in Fig. 9. The performed Fourier analysis showed that the distortions of the output signal are lower than 1%, which is in full compliance with the data given in [19]. The analysis shows clearly that these distortions are mainly caused by the second order harmonic, while the amplitudes of the higher order harmonics were lower than 0.01% in comparison with the amplitude of the fundamental.

V. Conclusions

The Spice model for the static induction transistor is presented. The model is based on the device behaviour rather than on the physical structure of the SIT. Simple method for model parameters extraction from the measured characteristics of the real SIT has been developed. Extensive simulations have been performed to examine the model characteristics. The model has passed all performed tests and the results correspond very well with the experimental ones given in [14], [15], [19] and [31]. Although the proposed model is not an ideal solution it will help to start simulating various circuits containing static induction transistors. The first problem to solve is the discrepancy between the measured and simulated curves for V_{gs} = 0, when simulating the high voltage devices, where the value of the internal diode resistance **rs** is relatively high. One possible solution is to add a small DC bias at the gate input of the model. This problem will be investigated in details in developing an advanced SIT model.

At least two other things are to be done in the near future: (1) to develop an algorithm for self extracting model parameters from devices data sheets; (2) to extend the model to covering both mode of SIT operation (triode and pentode-like) in order to enable full implementation of SIT for the Spice simulation program, or even to other circuit simulation program packages.

ACKNOWLEDGMENT

The author would like to thank the reviewers of this paper for their very constructive and useful comments and suggestions.

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