Modeling and Analysis of New Adaptive Dual Current Mode Control

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Abstract—**This paper proposes a new adaptive dual current mode control (ADCMC) approach which is modification of existing dual current mode control (DCMC). ADCMC introduces several significant advantages over DCMC, such as no peak-to-average error in the inductor-current signal, better transient response of inner current loop, improved line regulation and easier adjustment to different types of power electronics converters. Besides description of the working principles of ADCMC, this paper presents the development of small-signal model and transfer functions of ADCMC on the example of buck converter. Simulation results are presented which prove the derived analysis.**

Keywords- buck converter; current-mode control (CMC); line regulation; peak-to-average error; transient response.

I. INTRODUCTION

The control of power electronics converters can be divided into two main groups: voltage mode control (VMC) and current mode control (CMC). CMC is frequently used instead of VMC, because it has several important advantages over VMC. The one of them is overcurrent protection, for example. Further, it is well known that CMC improves converters' transient response by reducing the order of their transfer functions. Also, it improves line regulation by inherently built-in feed-forward property. CMC methods are first introduced in 1970s [1]. After that they have been increasingly used. Usually, CMC methods are divided into fixed-frequency and variable-frequency methods. In literature there are several basic fixed-frequency CMC methods and their modifications, including peak CMC (PCMC) [2]-[4], valley CMC (VCMC) [2], average CMC (ACMC) [5], [6] and charge control [7], [8].

PCMC and VCMC are the most commonly used among fixed-frequency methods. They have some excellent features, including constant switching frequency, simple implementation and good dynamic response. However, they have several drawbacks. The most important one is appearance of subharmonic oscillations when the duty cycle is above 0.5 (for PCMC) or below 0.5 (for VCMC) [9]. In order to eliminate these subharmonic oscillations, the slope compensation must be used. Also, they have large peak-to-average error in the inductor-current signal.

Variable-frequency CMC methods overcome these issues by operating in free-running mode. One of the most popular variable-frequency methods is hysteresis CMC [10], [11]. It has several advantages, including no slope compensation, no subharmonic oscillations and zero peak-to-average error. However, hysteresis CMC is not so suitable in practice due to its variable frequency. There are some modifications of hysteresis CMC, as in [12], [13], which rely on its fixed-frequency operation.

In [14] a fixed-frequency dual current mode control (DCMC) is proposed, which ensures stable operation of power converters for the entire range of duty cycle. Unlike PCMC and VCMC, DCMC needs dual boundaries (peak and valley) for the inductor current and two clock signals phase shifted for 180 degrees. In this way the converter naturally crosses from PCMC to VCMC and vice versa. DCMC is more complex to implement, but it offers important advantages, including no slope compensation, no subharmonic oscillations and fixed-frequency operation. However, DCMC has one important drawback. The gap voltage (width between two boundaries) must be chosen in advance properly to be larger than the maximum peak-to-peak ripple of the inductor current. This can adversely affect the waveforms of converter's inductor current and output voltage, especially in the cases of power factor correction circuits (PFC) and inverters, where peak-to-peak current ripple always changes during their work. Also, significant peak-to-average error exists.

This paper proposes a new adaptive dual current mode control (ADCMC), which improves the qualities of DCMC by introducing an adaptive gap voltage, which is equal to the measured instantaneous value of peak-to-peak current ripple. The result is close to hysteresis operation, but with fixed-frequency, which is ensured with two clock signals. ADCMC offers several advantages over DCMC which will be demonstrated in this paper.

This paper is organized as follows. ADCMC's principles of operation are presented in Section II. A small-signal model on the example of buck converter is developed in Section III. Section IV presents the simulation results. Finally, the conclusion is given in Section V.

II. PRINCIPLES OF OPERATION OF ADCMC

The basic principles of operation of DCMC proposed in [14] are presented in Fig. 1 for buck converter, along with characteristic operating modes. DCMC has two main parts: outer voltage loop (negative feedback with compensator $G_c(s)$ for regulation of output voltage v_o) and inner current loop (two comparators, clocks clk_A and clk_B and driving logic). The output of voltage compensator v_c is actually the reference inductor current. Upper and lower boundaries for the inductor current i_L are formed by summing and subtracting the control signal v_c with the voltage V_a. For correct and stable operation of DCMC the voltage band $2V_a$ must be larger than the maximum peak-to-peak ripple of the inductor current. Therefore, the voltage V_a must satisfy the following condition:

$$2V_a > K_{iL}\Delta i_{Lpp\max} = K_{iL}\frac{v_g}{4f_sL}, \tag{1}$$

where: K_{iL} is measuring gain and Δi_{Lppmax} is maximum peak-to-peak ripple of the inductor current, v_g is input voltage, $f_s=1/T_s$ is switching frequency and L is the inductor value.

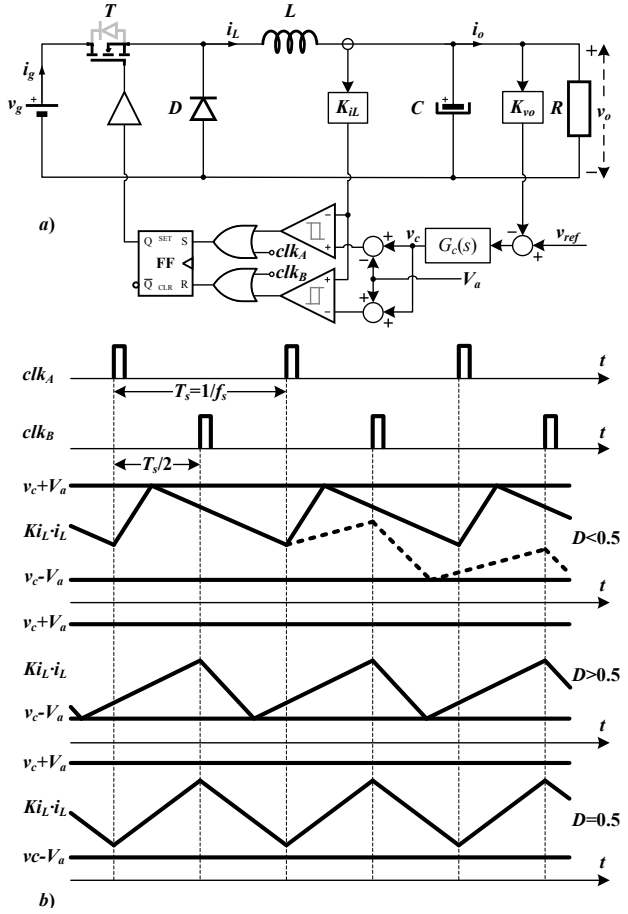

Figure 1. a) DCMC of buck converter, b) Characteristic operating modes.

It is obvious from Fig. 1.b (except for duty cycle D=0.5) that there is significant peak-to-average error in the inductor current (the difference between the reference current v_c and the average value of the inductor current), similarly as in PCMC and VCMC. Therefore, DCMC isn't able to directly control the average value of the inductor current. This can be an issue especially in PFC or inverter topologies. In these topologies with high voltage band $2V_a$ the transient response of the inductor current in boundary case (D=0.5) can be too slow, which results in distortion of waveforms of the inductor current and the output voltage. Also, every time when operating conditions change, such as input voltage, load, switching frequency, etc., a new value of voltage V_a must be determined.

In order to resolve these issues, this paper proposes a new ADCMC method, which is based on computation of voltage band $2V_a$ for the instantaneous operating conditions of converter. The voltage band $2V_a$ can be calculated using the instantaneous value of peak-to-peak current ripple Δi_{Lpp} in the following way:

$$2V_a = K_{va}K_{iL}\Delta i_{Lpp}, \tag{2}$$

where $K_{va}\geq 1$ is scaling factor. If K_{va}=1, ADCMC becomes similar to the hysteresis CMC, but with constant switching frequency. The great benefit from this feature is that ADCMC directly controls the average value of the inductor current, so no peak-to-average error exists. Also, the current transient response will be faster when some of the converter's parameters, especially input voltage, take sudden changes.

Equation (2) applies for general case regardless to the type of power converter. However, it is very difficult to directly measure the current ripple Δi_{Lpp}. It is commonly calculated by measuring the input and output voltage of converter. For the buck converter, the voltage band $2V_a$ is equal to:

$$2V_a = K_{va}K_{iL}\frac{v_o}{Lf_s}\left(1-\frac{v_o}{v_g}\right). \tag{3}$$

The scheme from Fig. 1.a remains the same for ADCMC.

III. SMALL-SIGNAL MODEL ANALYSIS

A small-signal AC model of the buck converter with ADCMC can be derived using standard procedure described in [15]. The small-signal averaged equations for buck converter from Fig. 1.a operating in the continuous conduction mode (CCM), under duty cycle control, can be expressed as:

$$\begin{aligned} L\frac{d\hat{i}_L(t)}{dt} &= D\hat{v}_g(t)-\hat{v}_o(t)+\hat{d}(t)V_g \\ C\frac{d\hat{v}_o(t)}{dt} &= \hat{i}_L(t)-\frac{\hat{v}_o(t)}{R} \\ \hat{i}_g(t) &= D\hat{i}_L(t)+\hat{d}(t)I_L, \end{aligned} \tag{4}$$

where $\hat{v}_g(t)$, $\hat{v}_o(t)$, $\hat{i}_g(t)$, $\hat{i}_L(t)$ and $\hat{d}(t)$ are small AC variations superimposed to the quiescent values V_g, V_o, I_g, I_L and D of input and output voltage, input and inductor current, and duty cycle, respectively. The quiescent values are equal to:

$$V = DV_g,\ I_L = \frac{V_o}{R},\ I_g = DI_L. \tag{5}$$

For modeling of ADCMC, a simple first-order approximation is employed, under assumption that the

measured average inductor current $K_{iL}\langle i_L(t)\rangle_{T_S}$ is equal to the reference current $v_c(t)$. This approximation is valid if the factor K_{va} is equal or approximate to one, while for DCMC this isn't the case. Using this approximation, following applies:

$$K_{iL}\hat{i}_L(t) = \hat{v}_c(t), \tag{6}$$

where $\hat{v}_c(t)$ is a small AC variation of current reference $v_c(t)$.

Substitution of (6) in (4) leads to the small-signal model of buck converter with ADCMC:

$$\begin{aligned} \frac{L}{K_{iL}}\frac{d\hat{v}_c(t)}{dt} &= D\hat{v}_g(t) - \hat{v}_o(t) + \hat{d}(t)V_g \\ C\frac{d\hat{v}_o(t)}{dt} &= \frac{\hat{v}_c(t)}{K_{iL}} - \frac{\hat{v}_o(t)}{R} \\ \hat{i}_g(t) &= \frac{D}{K_{iL}}\hat{v}_c(t) + \hat{d}(t)I_L. \end{aligned} \tag{7}$$

The Laplace transforms of (7) are:

$$\begin{aligned} \frac{L}{K_{iL}}s\hat{v}_c(s) &= D\hat{v}_g(s) - \hat{v}_o(s) + \hat{d}(s)V_g \\ Cs\hat{v}_o(s) &= \frac{\hat{v}_c(s)}{K_{iL}} - \frac{\hat{v}_o(s)}{R} \\ \hat{i}_g(s) &= \frac{D}{K_{iL}}\hat{v}_c(s) + \hat{d}(s)I_L. \end{aligned} \tag{8}$$

The control-to-output transfer function $G_{vc}(s)$ can be obtained from (8) as:

$$G_{vc}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\right|_{\hat{v}_g(s)=0} = \frac{R}{K_{iL}\left(1+sRC\right)}. \tag{9}$$

The simple transfer function (9) is used for design of the output voltage compensator $G_c(s)$. It is obvious from (8) that the line-to-output transfer function $G_{vg}(s) = \hat{v}_o(s)/\hat{v}_g(s)\big|_{\hat{v}_c(s)=0}$ is zero, which offers great line regulation. The identical transfer functions can be derived for DCMC, however due to the fact that the first-order approximation isn't valid for DCMC, the nonzero line-to-output transfer function exists, which is proved in [15] using a more accurate model.

IV. Simulation Results

The performances of ADCMC and its advantages over DCMC in the same operating conditions were tested with simulations for the buck converter with following parameters: V_g=28 V, L=120 μH, C=1000 μF, R=4 Ω and f_s=20 kHz. The all scaling and measuring gains K_{iL}, K_{va} and K_{vo} are set to one. According to (1) for DCMC the value of V_a was set to 2 V. The output voltage compensator $G_c(s)$ is a simple proportional-integral (PI) regulator. There will not be discussion about its design, because this paper is focused only on the inner current loop. Dynamics of the output voltage loop is too slow and doesn't affect the faster inner current loop.

A. Peak-to-average Error in Stationary State

In order to show the difference in peak-to-average error for DCMC and ADCMC, stationary state was analyzed for two values of the output voltage: 10 V and 20 V. The waveforms of inductor current, control signal, upper and lower current limit in stationary state are shown in Fig. 2 for DCMC and Fig. 3 for ADCMC.

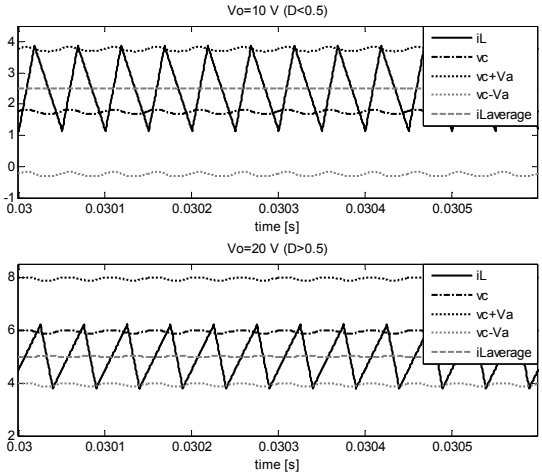

Figure 2. Simulation waveforms in stationary state for DCMC.

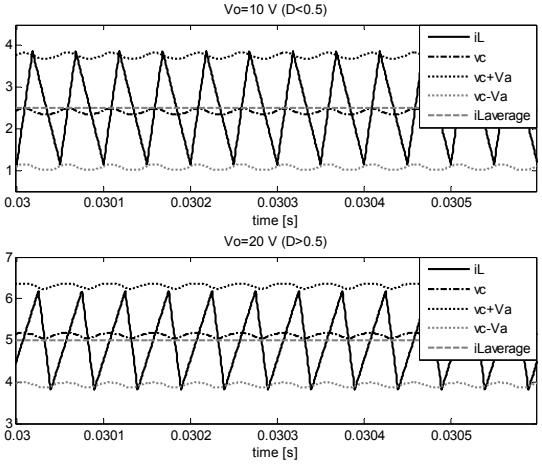

Figure 3. Simulation waveforms in stationary state for ADCMC.

It is obvious from Fig. 3 for ADCMC that the average value of the inductor current excellently follows the current reference (control signal v_c). However, if noted carefully, there is a small error between these two signals, which can be attributed to the delays in numerical calculation (simulation's solver) and fact that the voltage V_a from (3) applies for simplified model of buck converter in ideal conditions.

B. Line Regulation

Step changes of input voltage from 28 V to 16 V and vice versa are introduced in simulation in order to check the quality of line regulation of ADCMC. The output voltage was regulated to the value of 10 V. The results are shown in Fig. 4, Fig. 5 and Fig. 6.

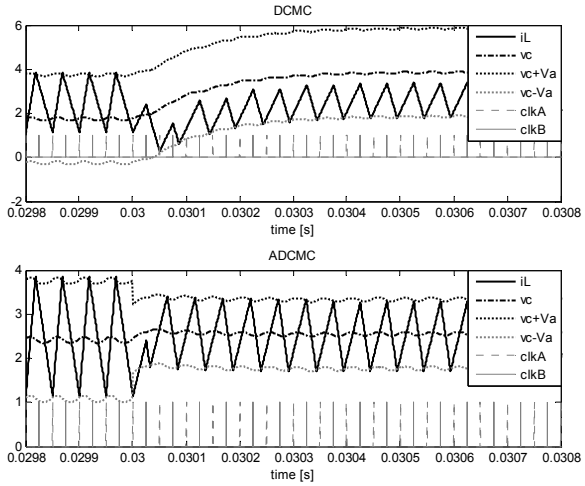

Figure 4. Simulation waveforms for a step change in the input voltage from 28 V to 16 V.

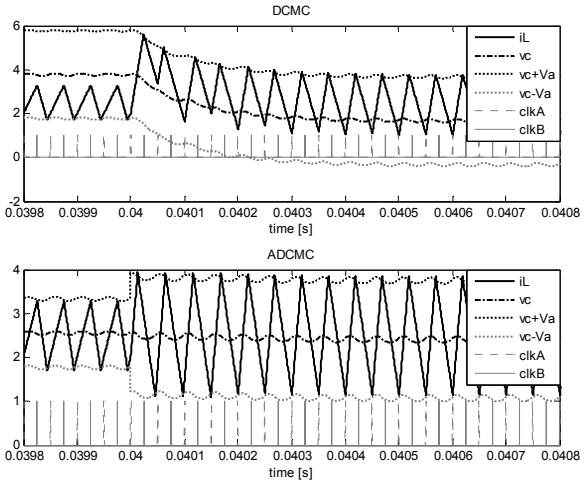

Figure 5. Simulation waveforms for a step change in the input voltage from 16 V to 28 V.

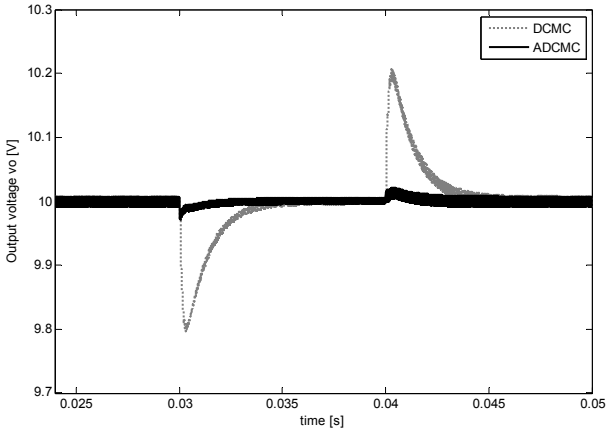

Figure 6. Output voltage for a step change in the input voltage from 28 V to 16 V and vice versa.

It is obvious from Fig. 4 and Fig. 5 that ADCMC has much better transient response of the inductor current, which results in a very improved line regulation, as shown in Fig. 6.

V. CONCLUSION

In this paper, a new adaptive dual current mode control method was proposed. A detailed analysis of ADCMC's principles of operation and small-signal model was presented. The performed simulations proved the analysis and showed some significant advantages of ADCMC over DCMC.

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