Bandgap Voltage Reference in 130nm: Design and Schematic Level Simulation

Aleksandar Pajkanovic
Faculty of Technical Sciences
University of Novi Sad
apaj@uns.ac.rs

Veljko Malbasa
Faculty of Technical Sciences
University of Novi Sad
malbasa@uns.ac.rs

***Abstract*—A bandgap voltage reference design based on a simple topology utilizing a current mirror and a complementary to absolute temperature voltage source is presented in the paper. Simulation results for implementation in 130 nm CMOS standard process show temperature variation of the output voltage within 5 mV over a temperature range of 165 K (from -40°C up to 125°C) in the nominal case, i.e. the absolute reference voltage temperature variation is 0.19 %, i.e. 11.5 ppm/°C. The influences of supply voltage and process variations (including corner and Monte Carlo analysis) on the output reference voltage are presented and discussed. Time domain analysis shows that the circuit is fully operational within 112 ns. The results are obtained through the schematic level simulations using Spectre Simulator from Cadence Design System.**

Keywords-CMOS, integrated circuits, bandgap, voltage reference, temperature stability

I. Introduction

The design of DC current and voltage sources internal to the chip is an essential step in monolithic integrated circuits design. The DC voltage and current references represent one of the basic blocks of analog electronics. Namely, the performance of nonlinear analog components depends strongly on the current flowing through them, i.e. biasing conditions. The task that these references should accomplish is to properly bias analog components of integrated circuits. Among a variety of solutions, efficient, simple and easy-to-design structures are the priority. These reference circuits should be autonomous when the supply voltage is switched on. Further, they should be based on intrinsic physical properties or on reproducible technology parameters [1], [2].

A process, voltage and temperature invariant reference voltage within an integrated circuits means stable biasing conditions - obtaining such a circuit for utilization in more complex systems is the main motivation for this work.

In this paper a simple topology is employed to design and simulate a bandgap voltage reference circuit intended to provide a temperature stable output voltage of around 1.2 V over a range from -40°C to 125°C. The technology process used is 130 nm, while the nominal supply voltage is 3.3 V and the design model is ACM model presented in [1]. The temperature coefficient achieved is 11.5 ppm/°C and the sensitivity of the reference voltage to the supply is 134 ppm/°C. Besides these, process variations are analyzed and treated through corner and Monte Carlo (statistical) analysis. Time response is also given to show that the circuit operates in a stable operating point, while the start-up time is 112 ns. The results listed are obtained through schematic level simulations using Spectre Simulator from Cadence Design System. In the end, the characteristics of this work are compared to several other such circuits found in literature and the possibilities of improvements are discussed.

II. Model Used

The design methodology is based on the ACM model [1], [3]. It is a current-based MOSFET model that uses the concept of inversion level. According to the ACM model, the drain current can be split into the forward (I_F) and reverse (I_R) currents:

$$I_D = I_F - I_R = I_S(i_f - i_r), \tag{1}$$

where I_S is the normalization specific current, and i_f and i_r are inversion levels, forward and reverse, respectively. The forward and reverse currents depend on the gate to source and gate to drain voltages, respectively. If the transistor operates in saturation, we have:

$$I_F \gg I_R, \text{ thus: } I_D \approx I_F = I_S \cdot i_f. \tag{2}$$

The normalization current is a function of the technology:

$$I_S = \frac{\mu C_{ox} \phi_T^2 n}{2} \frac{W}{L}, \tag{3}$$

where μ represents the charge mobility, C_{ox} gate-oxide capacitance per area, ϕ_T thermal voltage, n slope factor and W/L transistor aspect ratio.

The inversion level value signifies the transistor operation region in the following way: if $i_f < 1$, the transistor operates in weak inversion and if $i_f > 100$ the transistor operates in strong inversion region. If $1 < i_f < 100$, the transistor operates in moderate inversion region.

According to this model, the voltage and current are related in the following manner [1]:

$$\frac{V_P - V_{S(D)}}{\phi_T} = \sqrt{1 + i_{f(r)}} - 3 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right), \tag{4}$$

where V_P is the pinch-off voltage, given as the difference of the gate potential and the zero bias threshold voltage (modified by the slope factor):

$$V_P \approx \frac{V_G - V_{T0}}{n}, \text{ if } V_G \approx V_{T0}. \tag{5}$$

Further detailed description of the model can be found in [1] and [3].

III. Bandgap Voltage Reference Theory of Operation

A bandgap voltage reference operation is based on adding two voltages having equal and opposite temperature coefficients, i.e. a voltage proportional to absolute temperature (PTAT) and a voltage complementary to absolute temperature (CTAT). The logic behind this idea is to cancel out the temperature dependence, so that the output voltage, i.e. reference voltage is independent of temperature variation. Therefore, the reference voltage, V_{REF} we can write as:

$$V_{REF} = \alpha \cdot V_{CTAT} + \beta \cdot V_{PTAT}. \tag{6}$$

where α and β are coefficients of proportionality.

The temperature coefficient of a voltage is numerically expressed by the first derivative of that voltage as a function of temperature. Thus, in order to accomplish that V_{REF} is independent of temperature, its derivative needs to be zero:

$$\frac{\partial V_{REF}}{\partial T} = \alpha \frac{\partial V_{CTAT}}{\partial T} + \beta \frac{\partial V_{PTAT}}{\partial T} = 0. \tag{7}$$

To achieve this, a CTAT and a PTAT voltages need to be designed and, then, the coefficients α and β need to be set in such a way that slopes of these two voltages are equal.

The easiest way to obtain a CTAT voltage is the forward-biased pn junction - a diode. The diode current is given by [1]:

$$I_D = I_S \cdot e^{\frac{V_D}{\phi_T}}, \tag{8}$$

where I_S represents a diode saturation current and V_D is the diode voltage. From this relation, we extract the diode voltage as:

$$V_D = \phi_T \ln\left(\frac{I_D}{I_S}\right). \tag{9}$$

The two members comprising the expression for the diode voltage are of opposite temperature coefficient, but the PTAT (the thermal voltage) is negligible when compared to CTAT (the logarithm expression). Namely, the diode voltage temperature coefficient is given as [4]:

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)\,\phi_T - \frac{E_g}{q}}{T}, \tag{10}$$

where $m \approx -3/2$ is the exponential coefficient of the mobility dependence on temperature (expressed as $\mu \propto T^m$) and $E_g \approx 1.12$ eV represents the bandgap energy of silicon [4].

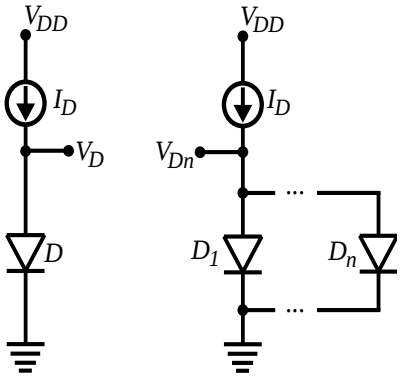

Figure 1. A PTAT voltage can be obtained as the difference of V_D and V_{Dn}

Therefore, the diode voltage is a CTAT in its nature. Assuming a standard value of $V_D = 0.75$ V and measuring at room temperature, (10) yields a temperature coefficient of around -1.5 mV/K.

To obtain a PTAT voltage, a pn junction is again used, i.e. several pn junctions are used. Namely, the idea is to subtract two V_D voltages, thus canceling the CTAT members and extracting the thermal voltage, i.e. the PTAT member. Such an effect can be obtained if there are different currents flowing through physically identical pn junctions, Fig. 1. Assuming an array of n identical diodes (Fig. 1), according to (9), the voltage of each one of them is given as:

$$V_{D1} = V_{D2} = ... = V_{Dn} = \phi_T \cdot \ln\left(\frac{I_D}{n \cdot I_S}\right). \tag{11}$$

Observing the difference of V_D and V_{Dn}, yields:

$$\begin{aligned} V_D - V_{Dn} &= \phi_T \cdot \ln\left(\frac{I_D}{I_S}\right) - \phi_T \cdot \ln\left(\frac{I_D}{n \cdot I_S}\right) \\ &= \phi_T \cdot \ln(n), \end{aligned} \tag{12}$$

which means that this voltage difference is PTAT in its nature.

The subtraction can be performed by inserting a resistor, as shown in Fig. 2. The voltage over R_1 is given as:

$$V_{R1} - V_{Dn} = I_D \cdot R_1. \tag{13}$$

If V_D and V_{R1} are equal, we can write:

$$V_{R1} - V_{Dn} = I_D \cdot R_1 = \phi_T \cdot \ln(n). \tag{14}$$

Therefore, in order for this idea to work, the current generators in Fig. 2 must be replaced by a circuit which will make sure that $V_D = V_{R1}$. In this circuit, the current I_D is completely determined by the resistor R_1.

There are different ways to provide equal voltage levels at points V_D and V_{R1}, including the application of a current mirror and an operational amplifier [1], [4]. Within this paper, the current mirror is used because of its simpler realization and a lower number of transistors. Thus, the ideal current generators in Fig. 2 are replaced by a current mirror, as shown in Fig. 3.

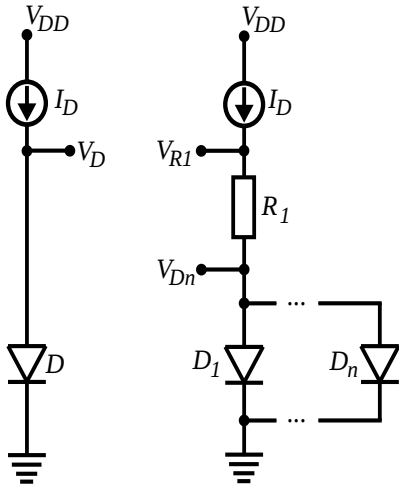

Figure 2. To obtain a PTAT, voltages V_D and V_{R1} must be equal

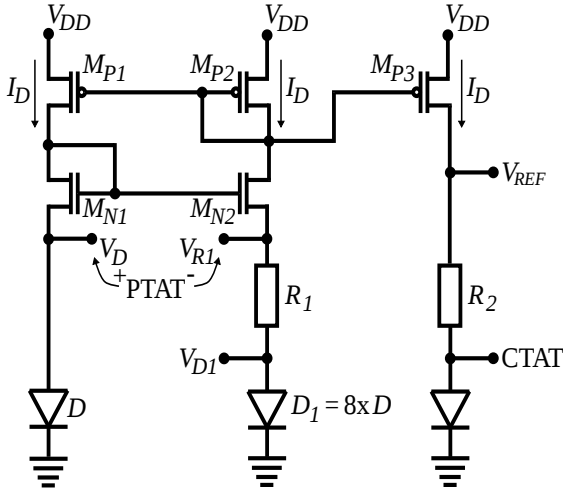

Figure 3. Proposed circuit schematic

The temperature coefficient of $V_{R1} - V_{Dn}$ is that of the thermal voltage:

$$\frac{\partial \phi_T}{\partial T} = \frac{k}{q} = 86.25 \frac{\mu \mathrm{V}}{\mathrm{K}}. \tag{15}$$

Now, both CTAT and PTAT voltages are provided, even though of unequal temperature coefficients. This issue is solved by setting the coefficients of proportionality, α and β, in the correct way. The last step is to sum these two voltages so that the whole circuit yields an output voltage constant to temperature variation. The easiest way to sum voltages is to simply connect them in series. This is what the third branch in Fig. 3 actually does. Namely, the output transistor, M_{P3}, copies the current from the current mirror. Thus, the voltage V_{REF} is given as:

$$V_{REF} = V_D + V_{R2} = V_D + I_D \cdot R_2. \tag{16}$$

From (14) we can write:

$$I_D = \frac{\phi_T \cdot \ln(n)}{R_1}, \tag{17}$$

which, used in (16), yields:

$$V_{REF} = V_D + \frac{R_2}{R_1} \cdot \ln(n) \cdot \phi_T. \tag{18}$$

Comparing this expression with (6), we realize the following identities: $V_{CTAT} = V_D$, $V_{PTAT} = \phi_T$ and $\alpha = 1$, $\beta = (R_2/R_1) \cdot \ln(n)$. Substituting according to these relations into (7), we obtain:

$$\frac{\partial V_D}{\partial T} + \frac{R_2}{R_1} \cdot \ln(n) \cdot \frac{\partial \phi_T}{\partial T} = 0. \tag{19}$$

Temperature coefficients of pn junction and thermal voltages are known from (10) and (15), respectively, whereas R_1, R_2 and n remain to be determined during circuit design.

IV. Circuit Design Using ACM Model

Some of the parameter values must be assumed. For example, since this is a DC circuit and it is of primary importance that all of the transistors be as equal as possible, we are allowed to choose a wide channel transistor - therefore, $W = 10$ μm. In this way, using larger transistors, matching is improved [4]. For the same reason, the number of parallel diodes in the second branch is chosen as $n = 8$. Namely, this means that there will be 9 diodes in the PTAT circuit, that can, thus, be positioned in a matrix of 3x3. In that way, all of the matching conditions will be fulfilled, and the probability of system mismatch highly lowered [4]. Further, a somewhat larger resistor is chosen, $R_1 = 1$ kΩ. Further, for the proposed circuit to function properly, all transistors must operate in saturation. Obviously, transistors M_{P1}, M_{P2} and M_{N1} will always operate in saturation, but for M_{N2}, this condition must be secured through component design. According to the ACM model, that means: $i_f \gg i_r$. To make sure that they will all remain saturated and in strong inversion in all cases, we assume $i_{f1} = 200$.

Using the transistor model approximate parameters, it is possible to calculate the sheet normalization current:

$$I_{SH} = \frac{I_S}{W/L} = \frac{\mu C_{ox} \phi_T^2 n}{2} = 61 \text{ nA}. \tag{20}$$

According to (17), the drain current, i.e. the current of each of the branches, is determined by the resistor R_1. Therefore, it can be calculated as $I_D \approx 53\mu$A. Now it is possible to calculate the transistor ratio:

$$\frac{W}{L} = \frac{53 \cdot 10^{-6}}{200 \cdot 61 \cdot 10^{-9}} = 4.4 \approx 5, \tag{21}$$

which means that $L = 2$ μm.

The final unknown value of this circuit is the resistivity of R_2, which is determined from the temperature invariance condition, (19). Even though an approximate value for $\partial V_D / \partial T$ is already mentioned in section III of this paper, it varies significantly for each technology. Therefore, the actual value of this coefficient for this particular technology process is obtained through an experiment: a simple DC simulation yields $\partial V_D / \partial T \approx -1.115$ mV/K, for the range of temperatures from -40 up to 125°C.

Substituting now the obtained temperature coefficients and the rest of the known values, we write an equation with only one unknown:

$$-1.115 \cdot 10^{-3} + \frac{R_2}{10^3} \cdot \ln 8 \cdot 86.25 \cdot 10^{-6} = 0, \qquad (22)$$

which provides a solution to the unknown value of the final circuit component, the resistor $R_2 \approx 6500\ \Omega$.

V. Simulation Results

Since we used approximate values for the calculations performed in section IV of this paper, some fine tuning is expected. After several iterations of simulations, these are the final parameter values of all the components used in circuit in Fig. 3 all transistor channel widths are 10 μm and all lengths are 2 μm, n =8 $R_1 = 1$ kΩ and $R_2 = 6.86$ kΩ.

In several simulations, the characteristics of the designed bandgap reference voltage circuit are demonstrated. First, the output of the circuit, i.e. the reference voltage, is shown as a function of temperature and of supply voltage. Then, process variations are simulated, observing the worst case scenarios through corner analysis and the statistical mismatch through Monte Carlo analysis. In the end, transient analysis is performed to show that the circuit's operating point is stable.

From Fig. 4 we see that the output voltage varies only $\pm$2.370 mV around the mean value of 1245.341 mV over a temperature range 160 K wide, i.e. from -40 to 125 °C. This is an error of 0.19 % and of 0.0012 % per °C, i.e. 11.5 ppm/°C.

Supply voltage variations are demonstrated in Fig. 5. The nominal value of V_{DD} is 3.3 V and here the circuit behavior at $\pm$10 % is shown. The simulation results show that, with the supply voltage change from 2.97 V to 3.63 V, the reference voltage changes its value within the border of $\pm$25.725 mV around the mean value of 1203.494 mV. Relative error is 2.14 % and 0.0134 % per °C, i.e. 134 ppm/°C.

In Figs. 6-9 process variations of the circuit in question are analyzed. Corner and Monte Carlo analysis are performed on top of temperature (Figs. 6 and 8) and on top of supply voltage (Figs. 7 and 9) variation analysis. Through corner analysis, worst case scenarios are treated, showing that the maximum possible change of the output voltage taking into account both temperature and process variations is around 30 mV, which is $\pm$1.24 %. Also, the maximum possible variation of the output voltage as a consequence of both supply and process variations is around 53 mV, i.e. $\pm$ 2.20 %.

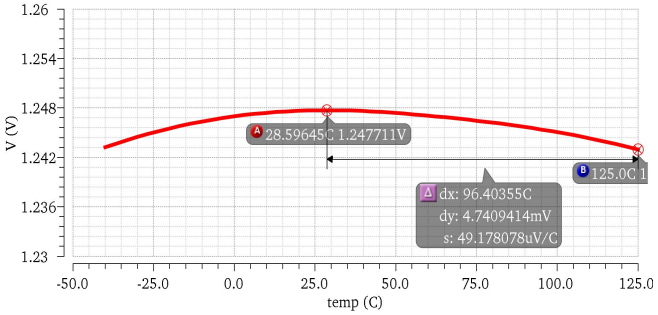

Figure 4. Temperature dependence of the output voltage at nominal supply voltage

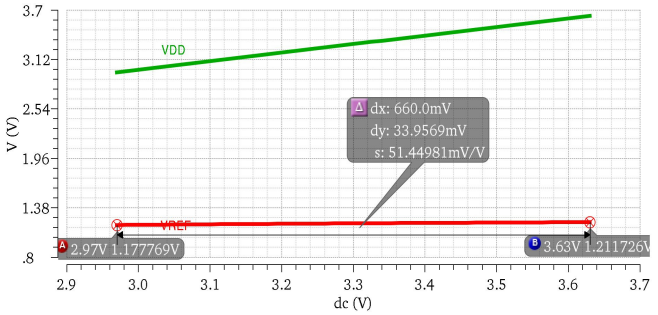

Figure 5. Output voltage dependence on the supply voltage

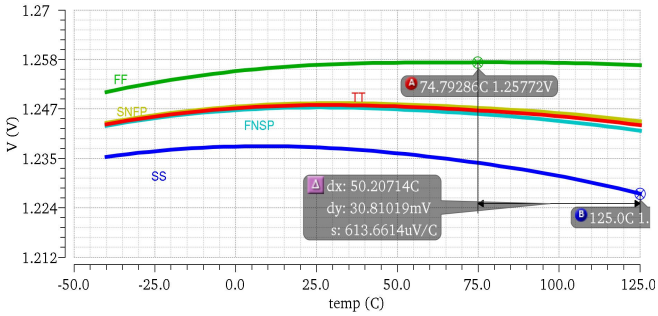

Figure 6. Corner analysis performed on top of the output voltage temperature dependence analysis

Statistical variations of the process are analyzed through Monte Carlo simulations, each with 30 iterations. According to the technology process documentation, statistical significance of 30 iterations is quite high. Namely, if the circuit operates correctly for all 30 runs, there is 99 % probability that over 80 % of all possible component values operate correctly. Statistical analysis performed on top of temperature analysis shows that the output voltage change is within $\pm$32.96 mV, which is $\pm$2.65 %, Fig 8. The same analysis performed on top of supply voltage analysis shows variance of the reference voltage within $\pm$49.34 mV, which is $\pm$4.10 % of the mean value, Fig. 9.

In Fig. 10 time response of the circuit with start-up circuitry added is shown. The addition does not influence DC operation of the circuit and it contains two PMOS transistors and a capacitor. Its purpose is to enable the operation of the bandgap reference voltage in its stable operating point [1]. The time domain analysis shows that the circuit provides nominal output voltage within 112 ns.

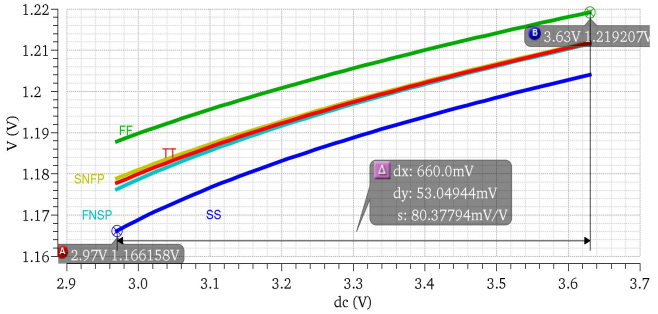

Figure 7. Corner analysis performed on top of a supply voltage analysis of the output voltage

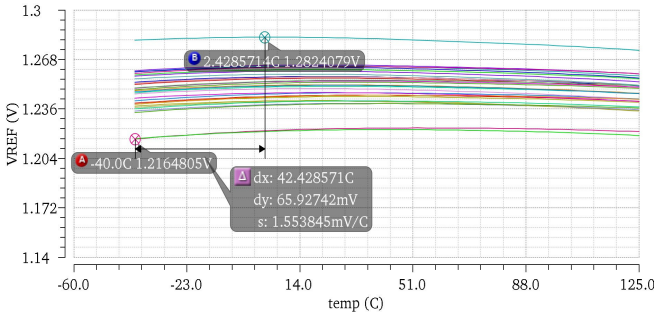

Figure 8. Statistical process variation observed through the Monte Carlo analysis of the temperature dependence of the output voltage

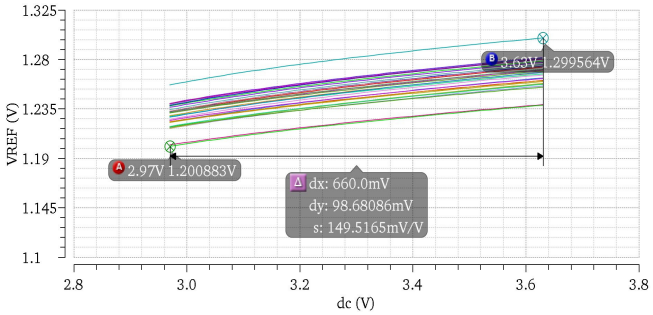

Figure 9. Statistical process variation observed through the Monte Carlo analysis of the output voltage dependence on the supply voltage

VI. Discussion

In Tab. I the characteristics of several circuits of the same purpose are compared. In [5] a bandgap voltage reference is implemented through a topology employing a current-voltage mirror instead of an amplifier, while in [6] a two-stage amplifier is used. These two are characterized by a somewhat larger temperature coefficient and lower power consumption, but at a narrower temperature range. Circuits presented in [7] and [8] show very weak variance of the reference voltage as a function of temperature over a wider temperature range. Also, these are characterized by higher power consumption, up to 1.3 mW. The topologies implemented use operational amplifier, with the addition of a 4-bit trimming circuit in [8]. The purpose of this additional circuit is to reduce the influence of the process variations.

The circuit presented in this paper shows temperature coefficient in the higher end of the shown scale, but of the same order of magnitude. In the context of power consumption, our work belongs in the middle with $P_D = 600\mu$W. Concerning topology, this is the simplest of those investigated, since it employs only a current mirror and a start-up circuit.

The circuit presented in this paper shows satisfying behavior concerning temperature variations. On the other hand, its supply voltage variation is larger. This is a consequence of a very simple circuit employed to force equal voltages V_D and V_{R2}. This current mirror's responsibility is to prevent the influence of supply voltage's disturbances of the output voltage, V_{REF}. A way to improve this feature of the circuit is to use an operational amplifier with extremely high gain in order to stabilize the noise coming from V_{DD}. In future work, such an attempt is to be made.

The purpose of this comparison in no way is a claim which of the circuits is better, since each one of them is designed with

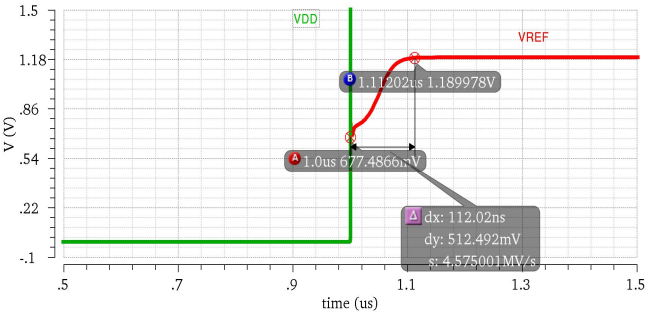

Figure 10. Time domain analysis, showing that the circuit starts-up in 112 ns

TABLE I. Characteristics comparison

Circuits	Technology process [nm]	Supply voltage [V]	Temperature coefficient [ppm/°C]	Temperature range [°C]	Power [μW]
[5]	350	2.5	12.1	5:95C	276
[6]	180	1.8	6.5	-20:90	150
[7]	130	3.3	5.5	-40:105	1300
[8]	180	1.8	2	-20:140	620
This work	130	3.3	11.5	-40:125	600

the author having a different goal in mind, e.g. low power, higher stability or smaller chip area. The Tab I is given in order to point out that the results obtained within this paper are of the same order like those found in current literature.

VII. Conclusion

A temperature stable bandgap reference voltage circuit is presented in this paper. Process variation analysis performed (both corner and Monte Carlo) show that the output is influenced by the fabrication process, and this characteristic remains to be worked upon during the layout phase, which follows. Supply voltage sensitivity is somewhat higher, but a way to improve this feature is given and is to be implemented in future work.

Acknowledgment

This work is funded from the European Union's Seventh Framework Program for research, technological development and demonstration under grant agreement no. 289481. - project SENSEIVER.

References

[1] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.

[2] T. Lee, *The RF CMOS Integrated Circuit Design*. Prentice Hall, 1998.

[3] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, 1998.

[4] B. Razavi, *Design of Analog CMOS Integrated Circuit*. McGraw-Hill, 2001.

[5] Y.-H. Lam and W.-H. Ki, "CMOS Bandgap References with Self-biased Symmetrically Matched Current-Voltage Mirror and Extension of Sub-1-V Design," *Very Large Scale Integrateion (VLSI) Systems, IEEE Transactions on*, vol. 18, no. 6, pp. 857–865, 2010.

[6] Y. Yusoff, H. C. Lah, N. Razali, S. N. Harun, and T. Yew, "Design and Characterization of Bandgap Voltage Reference," in *Semiconductor Electronics (ICSE), 10th IEEE International Conference on*, 2012, pp. 686–689.

[7] M. Lazic, D. Mirkovic, and P. Petkovic, "Integrated Voltage Reference Design in 130 nm CMOS Technology Process (in Serbian)," in *Proceedings of 57th ETRAN Conference, Zlatibor, Serbia*, 2013, pp. EL2.1.1–6.

[8] A. Martinez-Nieto, M. Sanz-Pascual, P. Rosales-Quintero, and S. Celma, "A Bandgap Voltage Reference in 0.18μm CMOS Technology," in *Circuits and Systems (MWSCAS), IEEE 56th International Midwest Symposium on*, 2013, pp. 97–100.